Keywords: 21-bit multiple input channel deserializers, skew margin measurement, jitter tolerance, clock jitter, data jitter, channel-to-channel skew, DC balance

APPLICATION NOTE 3821

Skew Margin Measurement for 4-Channel (3 Data Channels Plus Clock Channel) LVDS Serializers/Deserializers

Jun 20, 2006

Abstract: Measuring receiver skew margin is a practical way to determine the jitter tolerance of multiple-input-channel LVDS deserializers like the MAX9209/MAX9222 parts. Although receiver skew margin has been defined and explained in the literature, no comprehensive measurement technique has yet been demonstrated. This application note shows a step-by-step method for measuring skew margin. Following this approach, you can clarify the specification and definition of skew margin in the data sheets for these 4-channel SerDes devices.

The following measurements were performed in several steps and using the MAX9209/MAX9222 serializer/deserializer (SerDes) parts in DC-balance mode with a 10m shielded twisted-pair cable. In all measurements, a Tektronix P6248 FET differential probe and a Tektronix CSA8000 sampling oscilloscope were used. A PRBS data pattern was used.

Step 1

Make the peak-to-peak jitter measurement at 0V differential on the rising edge of RxCLKIN. Call it Tjclk. (See **Figure 1**.)

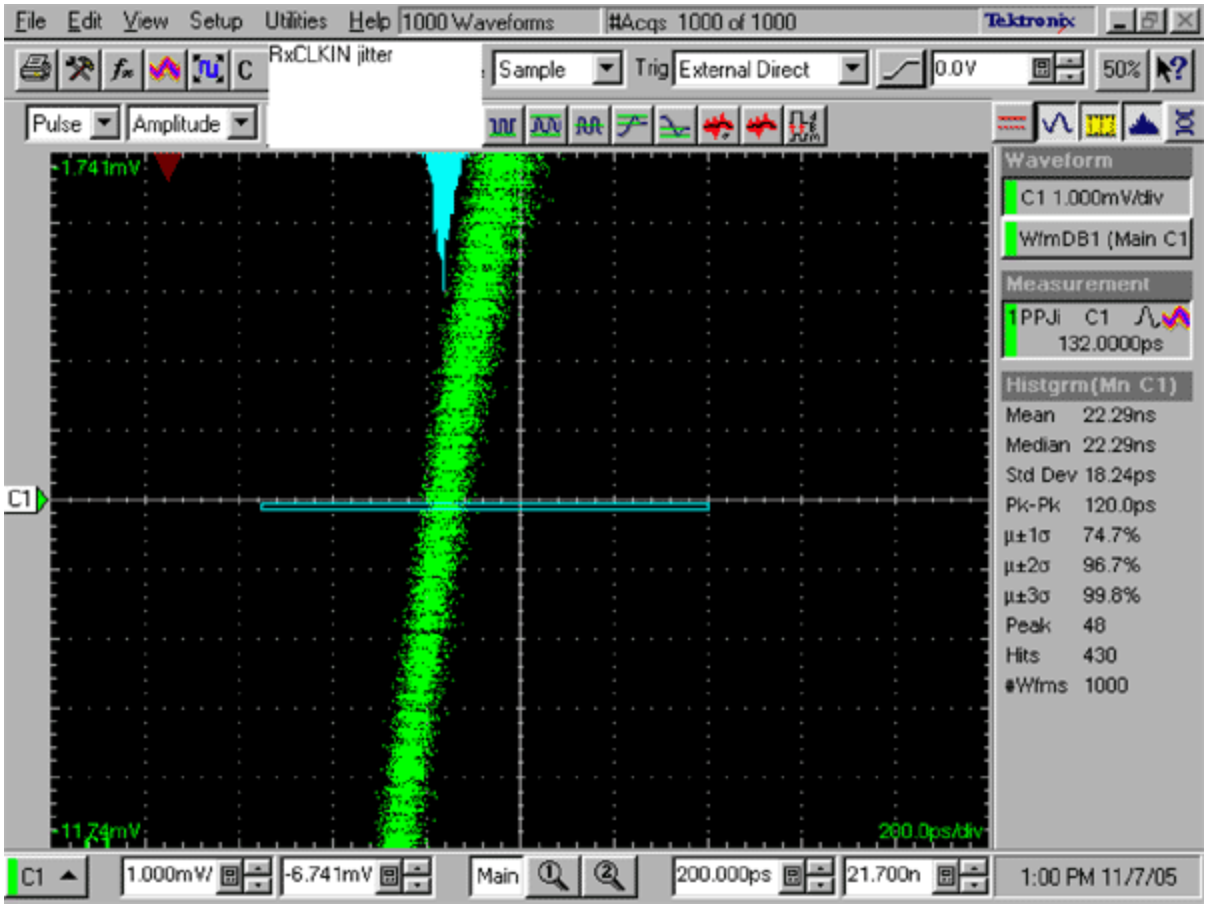

Figure 1. Clock jitter measurement at 0V differential.

Step 2

Measure the time difference (skew) between the rising edge of RxCLKIN and the leading edge of the serial DCA bit for each LVDS data channel at the MAX9222 input. (See Figure 10 in the MAX9222 data sheet.) There will be three measurements. Call them Tsk0, Tsk1, and Tsk2. (See **Figure 2** below.)

These skew measurements should be made from the center point of the jitter on RxCLKIN to the center point of the jitter on each LVDS data input. As shown in Figure 10 of the data sheet, ideally the rising edge of RxCLKIN aligns with the leading transition of the DCA bits. Skew is the departure from this ideal. This skew derives mainly from path-length differences between LVDS channels.

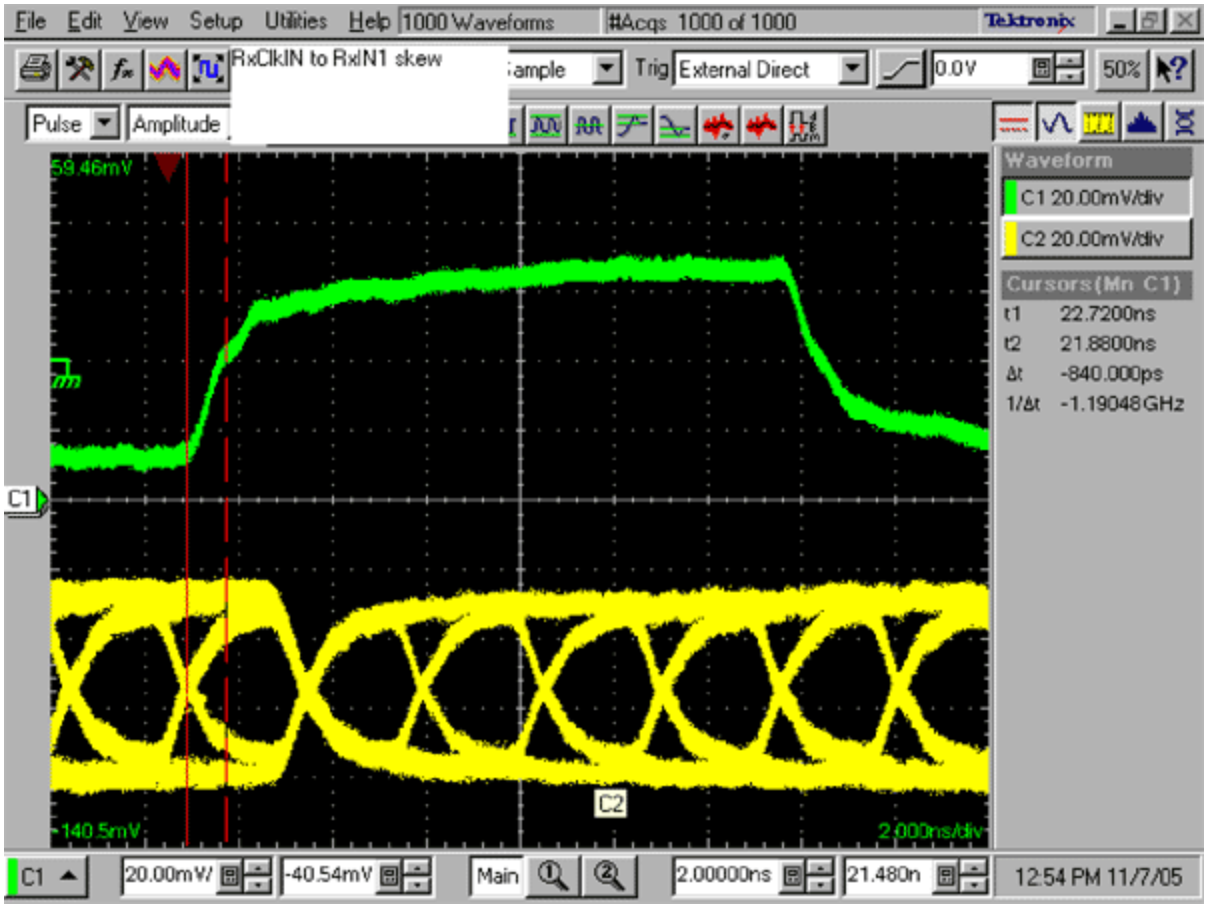

Figure 2. Clock-to-data skew measurement taken on a MAX9222 serializer.

Step 3

Measure the peak-to-peak jitter at differential zero of the transitions for each serial bit on the LVDS data channels RxIN0, RxIN1, and RxIN2. (See Figure 13 in the MAX9222 data sheet).

You will need to use the PRBS generated by the MAX9209. To generate the PRBS data, pull pin 14 and pin 27 of the MAX9209 low, and apply a clock to the MAX9209 TxCLKIN. Alternatively, applying moving picture video or a complex test pattern can be used as a rough check.

There will be 27 total measurements. Call them Tjd1-Tjd27. To speed the measurements, only a few bits with the highest peak-to-peak jitter are visually selected and measured (see **Figure 3**).

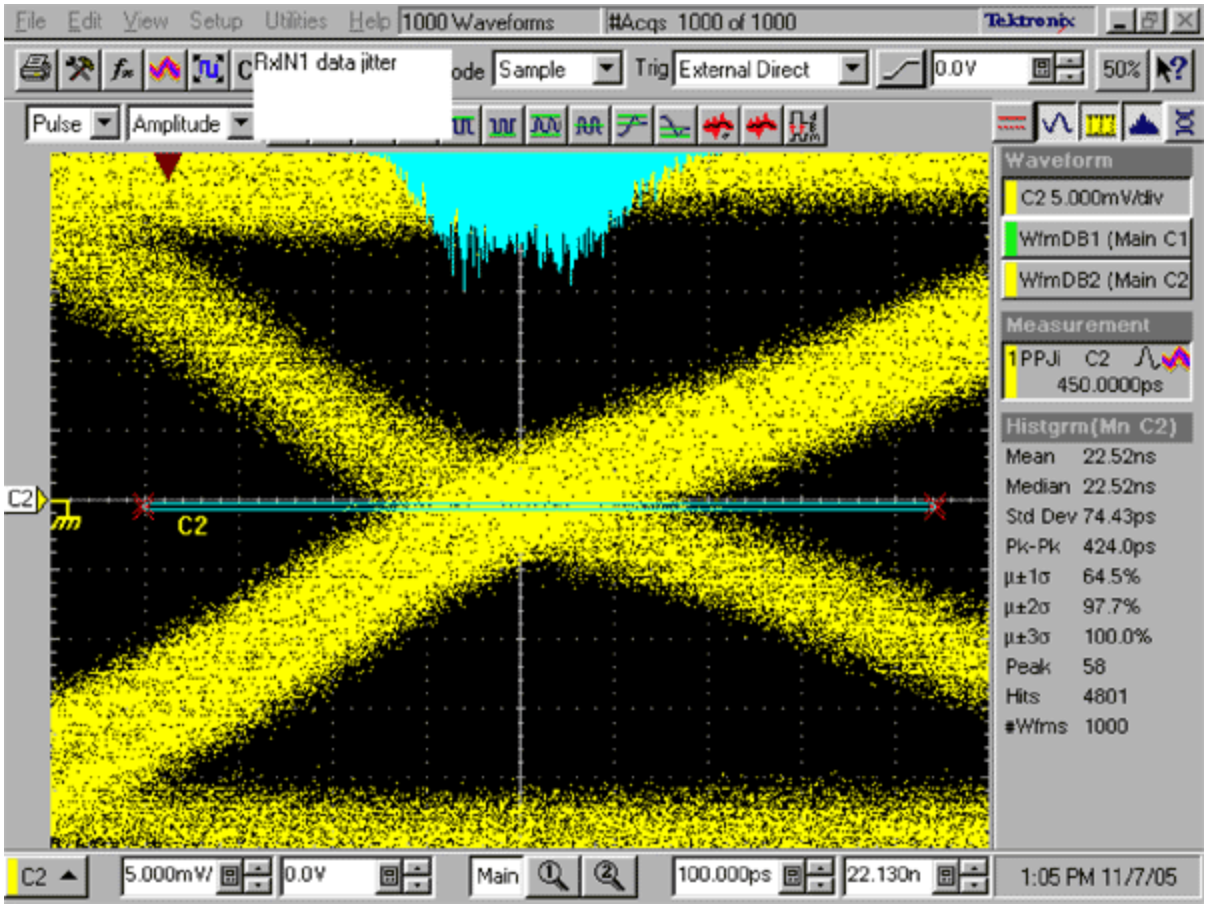

Figure 3. Data jitter measurement.

Step 4

Identify the largest data jitter among Tjd1-Tjd27, and call it TjdL.

Step 5

Identify the largest skew value among Tsk0, Tsk1, and Tsk2, and call it TskL.

Step 6

To meet the skew margin specification (RSKM in the MAX9222 data sheet), the following equation must be true:

RSKM ≥ (TjdL / 2) + ((Tjclk / 2) - 75ps) + TskL

75ps is half of the 150ps assumed for the MAX9209 serializer's pulse position variation. (See Note 6 in the MAX9222 data sheet.)

The method presented in the application note agrees with the specifications, figures, and explanations in the MAX9222 data sheet.

Related Parts		
MAX9209	Programmable DC-Balanced 21-Bit Serializers	Free Samples
MAX9214	Programmable DC-Balance 21-Bit Deserializers	Free Samples
MAX9222	Programmable DC-Balance 21-Bit Deserializers	
MAX9238	Hot-Swappable, 21-Bit, DC-Balanced LVDS Deserializers	
MAX9242	21-Bit Deserializers with Programmable Spread Spectrum and DC Balance	Free Samples
MAX9244	21-Bit Deserializers with Programmable Spread Spectrum and DC Balance	Free Samples
MAX9246	21-Bit Deserializers with Programmable Spread Spectrum and DC Balance	Free Samples

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